Science Bulletin 68 (2023) 787–790

Contents lists available at ScienceDirect

Science Bulletin

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Perspective

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Identifying proper metallic interfaces for two-dimensional (2D) semiconducting materials, with an Ohmic contact that is as electrically less resistive as possible, has long been a dream in 2D nanoelectronics [1,2]. In recent years, 2D semiconductors, especially transition metal dichalcogenides (TMDs) including WS_2, WSe_2, and MoS_2, have developed rapidly from standalone devices to the construction of integrated circuits at a scale of hundreds of logic gates [3]. However, the performance of most of these devices has not yet reached their intrinsic physical limits, as their electrode-semiconductor interfaces often have a contact barrier that is even more pronounced at low temperatures. The lack of a good contact has not only hindered the potential applications of room temperature electronics of 2D semiconductors, but also the fundamental physics at their ground states. For example, TMD monolayers can manifest a rich set of fractional quantum Hall gaps under magnetic field at a few Kelvin [4], but these fascinating properties have never been successfully demonstrated using electrical transport measurement due to contact barriers at low temperatures.

A Schottky barrier forms when a semiconductor and a metal are interfaced, leading to a nonlinear *I*–*V* curve and elevated resistance at low bias. To mitigate this, ion-implantation, as well as specific wiring techniques, has been developed in the silicon industry, achieving very low contact resistances (less than 200 Ω μm) and reliable circuitries. Along with high reproducibility, controllable doping, and self-oxidized gate dielectric, these advancements have made it extremely challenging to compete with silicon technology using other semiconducting materials.

Just like Si semiconductors, 2D semiconductor logic devices also adopt the famed metal–oxidesemiconductor field-effect-transistor (MOSFET) architecture. A van der Waals (vdW) layered semiconductor channel (as thin as a single layer) is placed on an insulating substrate, with the source-drain electrodes connecting the 2D semiconductor channel (which can be a flat film or a standing fin structure) with the external circuit, and the gate electrode regulating the carrier concentration of the semiconductor channel through a dielectric layer.

However, unlike Si semiconductors, achieving Ohmic contact with 2D semiconductors is difficult mainly because 2D vdW materials have an ultrathin thickness and an inert surface without dangling bonds, while there is a vdW gap between layers. In general, the contact of 2D semiconductor materials can be categorized into three fundamental types: (1) surface contact with a vdW gap, (2) surface contact without vdW gaps (with hybridization), and (3) one-dimensional (1D) edge contact, as shown in Fig. 1. On one hand, hybridization between the electrode and 2D semiconductors by sputtering or evaporation often destroys the crystal structure of the semiconductor channel itself. These chemical disorders and Fermi level pinning (or metal-induced gap states) hence lead to deteriorations in the current-delivery capability [5,6]. On the other hand, even in the scenario of clean contact where hybridization is absent between the electrode and 2D semiconductors, there will still be a vdW gap in addition to the Schottky barrier (Fig. 1d).

To date, various methods have been attempted to reduce the contact barriers in metal-2D semiconductor (M-2DS) interfaces within the three schemes mentioned above. However, obtaining a universal method for addressing the contact problem in 2D semiconductors remains challenging due to the difficulty of simultaneously achieving a zero or negative Schottky barrier, phase coherence of electrons across the interface without backscattering, and elimination of the vdW gap. Nonetheless, recent advances suggest that there are strategies that can help achieve contact approaching the quantum limit almost perfectly. These strategies will be further discussed in the following text.

In the following, representative works are highlighted in a timeline over the past decade, from 2014 to the present (Fig. 2a), for the research progress of an M-2DS interface.

Phase-engineered contacts (2014). Some of the 2D semiconducting materials have different crystallographic phases that can switch from semiconducting to metallic at a rather low energy cost. This metallic part can then become a transition section for electrical contact, reducing the Schottky barrier due to the covalent bonding between the heterophase of the same stoichiometric composition. Reports have shown that phase engineering can be one method of achieving Ohmic contact with 2D semiconductors such as $MoTe_2$ and MoS_2 [7,8].

Graphene/graphite 2D contacts (2015). 2D materials are often encapsulated with hexagonal boron nitride (h-BN) to obtain clean and atomically flat channels, which are then bridged using a 1D edge contact [9]. Although very efficient for electrical contacts to graphene/h-BN sandwiches, the 1D edge contact is not effective for ultrathin 2D TMD semiconductors, probably due to the high

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https://doi.org/10.1016/j.scib.2023.03.044

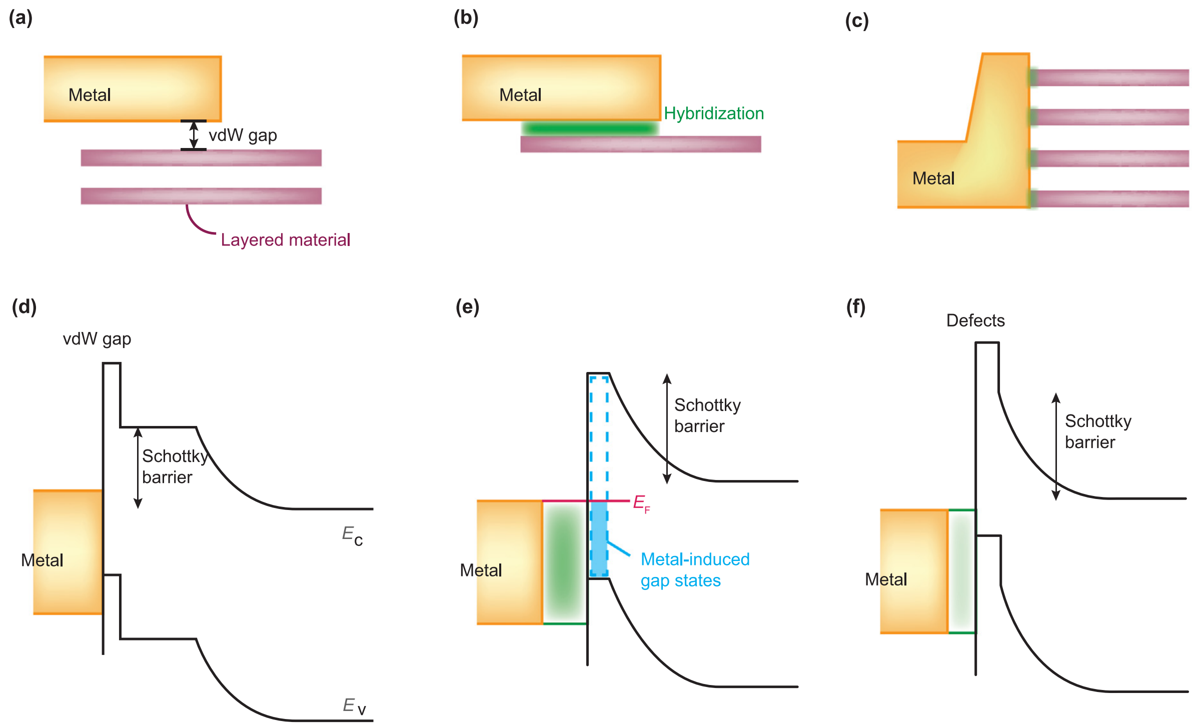

Fig. 1. (Color online) Three fundamental types of contacts to 2D semiconductor materials, including (a) surface contact with a vdW gap, which acts as an additional tunnel barrier before the inherent Schottky barrier [1]. (b) surface contact with hybridization, and (c) 1D edge contact, while (d)–(f) are schematics of their corresponding band alignment.

density of defects at the 1D edge, which yields non-linear *I*–*V* curves, especially at low temperatures. Studies using few-layered graphene or graphite flakes as electrodes to contact MoS_2 have shown much-improved transport performance and remarkable quantum Hall signatures [10].

Partially etched contacts (2016). A delicate partial etching method was developed in 2016 to achieve an Ohmic contact by evaporating metal through a window opened in the encapsulating h-BN layer above the 2D semiconductor channel. This improvement in contact has recently been shown to originate from the effective engineering of interfacial bonding distortion in TMDs, leading to substantially increased carrier-injection efficiency [11].

Tunnel contacts (2017). When the tunneling barrier and band offset are fine-tuned at the M-2DS interface, the electrical contact can also be significantly improved. For instance, a Co electrode evaporated onto a TMD channel with a monolayer h-BN spacing layer can yield rather linear *I*–*V* curves and a low-*T* contact resistance as low as 3 kΩ μm at a carrier density of $5.3 \times 10^{12}/cm^2$ [12]. The key role of monolayer h-BN here is to modify the work function of Co and simultaneously act as a tunneling barrier.

Evaporated electrodes vs. peel-&-transferred electrodes (2018). A peel-and-transfer method was proposed to laminate pre-patterned metal electrodes, with their work function matching the conduction band or valence band edges of the target 2D semiconductor. It thus avoids the ruptures and defects caused by metal evaporation/sputtering, approaching the Schottky-Mott limit in M-2DS junctions [5]. Notably, the polarity of a MoS_2 field-effect transistor (FET) can also be modulated using this method, in comparison to their counterparts by conventional evaporation, whether Pt-contacted p-type or Ag-contacted *n*-type.

Indium contacts (2019). Finding a metal that exhibits an ideal band offset between it and the 2D semiconductor with zero Schottky barrier can be a solution, but this has remained unclear until 2019 when near-ideal band offsets and defect-free interfaces were reported in NbS_2, WS_2, and WSe_2 when contacted with an indium alloy [13]. The lowest contact resistance of (220 ± 50) Ω μm on ultrathin NbS_2 was achieved.

Thermal scanning probe lithography (t-SPL) (2019). The *t*-SPL technique utilizes a heated scanning probe that can locally evaporate the polyphthalaldehyde (PPA) resist, allowing for simultaneous lithography and imaging without the need for vacuum conditions [14]. The key advantage of the technique is the elimination of resist contamination and damage caused by electron radiation, which are commonly encountered in conventional electron beam lithography. The tested MoS_2 FETs exhibit low Schottky barrier heights (~ 0 mV), high on/off ratios (10^{10}), and a subthreshold swing of 64 mV/dec. Linear *I*–*V* curves can be obtained even at low temperatures down to 48 K, with the contact resistance at the order of a few kΩ μm.

Pt or Au bottom electrodes (2020). Several research groups found that pre-patterned Pt or Au electrodes serving as bottom electrodes may significantly improve the M-2DS interface, preferably with the cleaned Pt or Au surface and the sample-fabrication in a glove box under an inert atmosphere [15]. It thus opened more accessibilities to probe quantum transport behaviors at the ground state [15,16].

Bismuth contacts (2021). Another approach to achieve a zero Schottky barrier height is to use semimetallic bismuth as the contact to semiconducting monolayer MoS_2. In this scheme, the metal-induced gap states are suppressed and degenerate states in the MoS_2 are spontaneously formed in contact with bismuth [6]. It thus leads to an on-state current density of 1.135 mA/μm on monolayer MoS_2 and a contact resistance of 123 Ω μm, approaching the quantum limit of contact resistance, defined as $R_C^{limit} = \pi R_Q / 2|\boldsymbol{k}_F| \approx 0.036(n_{2D})^{-0.5}$ kΩ μm, where $\boldsymbol{k}_F$ is the Fermi wavevector (for an isotropic Fermi surface) and $R_Q = h/e^2$ is the quantum resistance with *h* being the Planck's constant and *e* the elementary charge.

Selenium buffer layer (2022). By introducing a selenium buffer layer, which is later evaporated in an annealing process, contacts with a cleaner interface through a vdW gap to 2D semiconductor

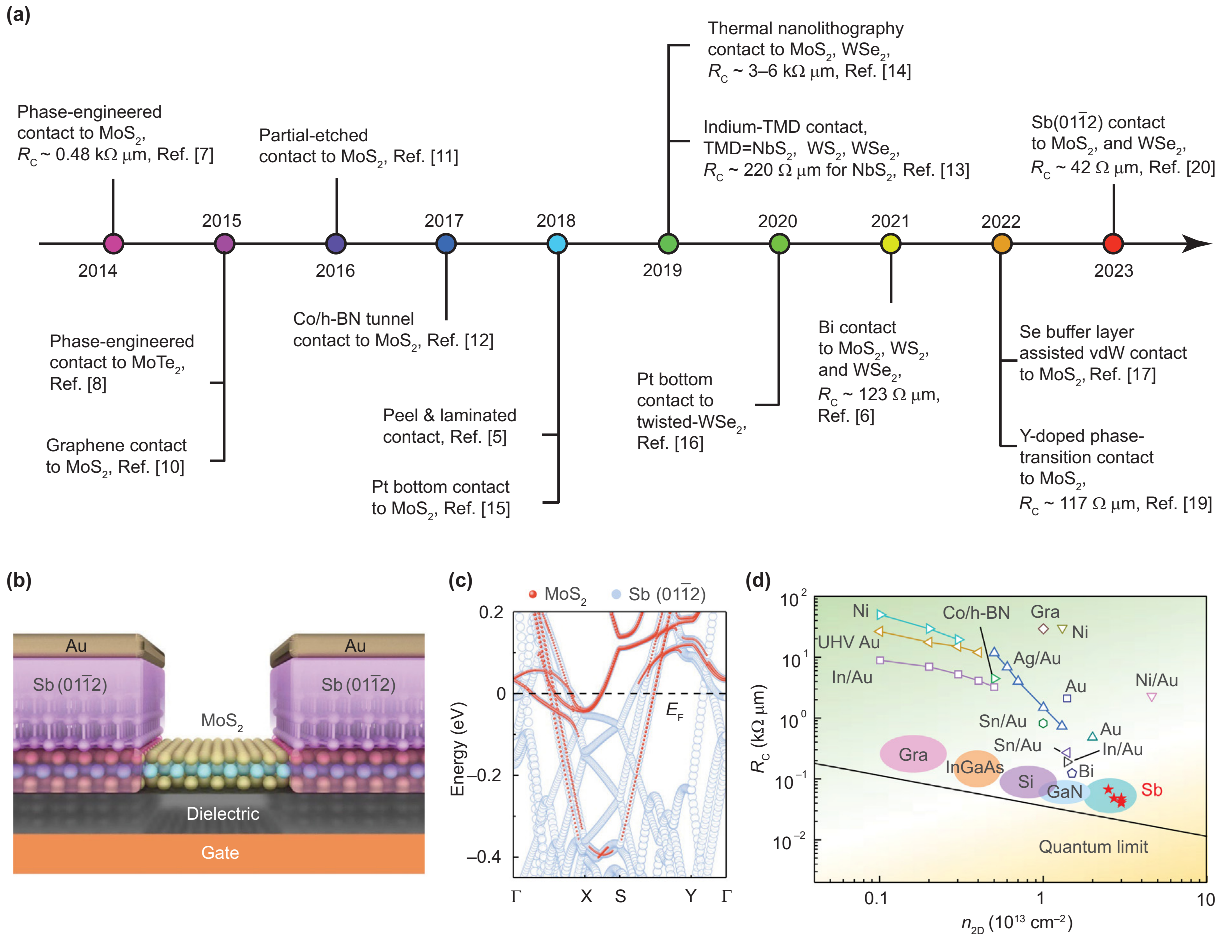

Fig. 2. (Color online) (a) Representative works in a timeline from 2014 to 2023 for the research progresses of M-2DS contacts. (b) Schematic picture of a FET device of Sb (01$\bar{1}$2)-contacted MoS_2. (c) Band hybridization of Sb (01$\bar{1}$2)-MoS_2 interface. (d) Summarization of MoS_2 contact resistance as well as some other semiconductors (graphene, InGaAs, Si, and GaN). Images in (b)–(d) are adopted from Ref. [20].

can be achieved. This method can produce high quality FET. Notably, p-type WSe_2 field-effect transistors with such vdW-Au contact exhibit outstanding properties, including stable operation with on/off ratio of 10^6, mobility of 155 $cm^2/(V\ s)$, contact resistance of 1.25 kΩ μm, and Schottky barrier height of 60 meV [17]. We came to notice that similar idea was also adopted in a recent work, using polymethyl methacrylate (PMMA) resist as a buffer layer toward improved contacts to 2D semiconductors [18].

Elemental-doping induced phase transition (2022). Similar to the approach of phase-engineered contact to 2D semiconductors, elemental doping of the 2D semiconducting channel at the contact region can effectively induce a semiconductor-to-metal phase transition, leading to a reduction in the Schottky barrier height. Recent studies have shown that when the top layer of S-atoms in 2H-phase MoS_2 is substituted with Yttrium atoms, it can be transformed into a metallic Y-1T'-phase, resulting in nearly ideal Ohmic contact and significantly improved transistor performance [19].

Antimony contacts (2023). Recently, researchers have found that low-melting point semimetallic Sb can also be a promising candidate for electrical contact with 2D semiconductors (Fig. 2b–d). Calculations suggest that, in contrast to other surfaces such as Sb (0001), the Sb(01$\bar{1}$2)-MoS_2 contact exhibits much stronger interlayer band hybridization due to the overlap between the Sb p_z orbital and the Mo d orbital, as well as a small tunnel barrier width of 1.35 Å [20]. In particular, charge transfer between Sb(01$\bar{1}$2)-MoS_2 pulls the MoS_2 conduction band minimum 0.4 eV below its Fermi level, which favors the Ohmic contact. Compared to the Bi contact, the Sb(01$\bar{1}$2) contact (obtained by heating the substrate to 100 ℃ during thermal evaporation) has contact resistance even closer to the quantum limit (42 Ω μm), yet with higher thermal stability, faster electrical operation speed, and more homogeneous performance over a millimeter scale. It is worth noting that, in the two methods of achieving near-quantum-limit M–SC contacts [6,20], Sb has a higher melting point than Bi (Sb ~ 630 ℃, and Bi ~ 271 ℃) and is therefore more compatible with the back-end CMOS process. Indeed, Sb contact technology has so far shown the most excellent properties in terms of reliability, device performance, and uniformity, holding great promise for future applications in 2D semiconducting nanoelectronics.

To conclude, nowadays, along with the booming in the research field, keeping 2D semiconducting materials in good contact with metallic electrodes is of paramount importance and urgency for large-scale integrated circuitry. Furthermore, Ohmic contacts for 2D semiconductors are not only crucial for room temperature nano-electronic applications, but also to reveal fundamental physical properties at their quantum ground states at very low temperatures. However, it is important to emphasize that there are still several technical challenges that need to be addressed in the longer-term perspective for the implementation of 2D semiconductors in future nanodevices at a large scale. These challenges include heat dissipation, controllable p- and n-doping, large-area uniformity suitable for industrial production, and vertical multilayer 3D interconnection of 2D logic. For each of these technological advancements, the search for perfect contacts to 2D semiconductors will undoubtedly continue.

Conflict of interest

The author declares that he has no conflict of interest.

Acknowledgments

The author acknowledges helpful discussions from Profs. Jianhao Chen, Teng Yang, and Yu Ye.

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